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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,082	11/26/2003	Masahiro Kiyotoshi	04329.3186	7869
22852	7590	08/05/2005	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			LEE, EUGENE	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/721,082

Applicant(s)

KIYOTOSHI, MASAHIRO

Examiner

Eugene Lee

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-15 is/are pending in the application.
- 4a) Of the above claim(s) 8,9 and 11-15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-7 and 10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4/26/05.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 6, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim 6,617,628 B2. Kim discloses (see, for example, Fig. 5B) a ferroelectric memory device comprising a semiconductor substrate 10, stack capacitor (capacitor structure) comprising an upper electrode layer (first electrode) 69, middle electrode layer (second electrode) 67, lower electrode layer (third electrode) 65, ferroelectric layer (first dielectric film) 68, ferroelectric layer (second dielectric film) 66, insulating layer (insulating film) 72, first hole, second hole, third hole, metal interconnection (first conductive connection) 73, and plate line (second conductive connection) 76.

Regarding the limitation “wherein an outer end of the second electrode is entirely positioned outside the first electrode in a direction parallel to a main surface of the semiconductor substrate and an outer end of the third electrode is entirely positioned outside the second electrode in the direction parallel to the main surface of the semiconductor substrate”, see, for example, FIG. 5B wherein Kim discloses left end (outer end) of middle electrode layer 67 being positioned outside the upper electrode layer 69; and the right end (outer end) of lower electrode layer 65 being positioned outside the middle electrode layer 67.

Art Unit: 2815

Regarding claim 6, see, for example, column 5, lines 38-43, wherein Kim discloses the ferroelectric layers (same material) being lead zirconia titanate (PZT), lead lanthanum zirconia titanate (PLZT), strontium barium titanate (SBT), and barium lanthanum titanate (BLT).

Regarding claim 7, see, for example, column 5, lines 25-58, wherein Kim discloses the electrode layers (same material) being platinum, iridium oxide, ruthenium oxide, and LaSrCo oxide (LSCO).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3 thru 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim '628 B2 as applied to claims 1, 6, and 7 above, and further in view of Kasahara 6,340,832 B2. Kim does not disclose a ring-shaped electrode surrounding the first electrode. However, Kasahara discloses (see, for example, FIG. 5B) a semiconductor device comprising a lead electrode (first electrode) 9, and a lead electrode (ring-shaped electrode) 8a, 8b. In the abstract, Kasahara discloses that capacitance error and phase rotation in a high frequency can be reduced. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a ring-shaped electrode surrounding the first electrode in order to reduce capacitance error and phase rotation in a high frequency.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim '628 B2 as applied to claims 1, 6, and 7 above, and further in view of Azuma et al. 5,814,849. Kim does not disclose a wiring metal layer provided between the semiconductor substrate and the capacitor structure. However, Azuma discloses (see, for example, FIG. 1) an integrated circuit 19 comprising an adhesion layer (wiring metal layer) 13, capacitor 10, and silicon wafer (substrate) 11. In column 3, lines 3-4, Azuma discloses the adhesion layer comprising titanium (metal). The adhesion layer adheres the first electrode layer 14 of the capacitor to the silicon wafer. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a wiring metal layer provided between the semiconductor substrate and the capacitor structure in order to adhere the electrode layer to the semiconductor substrate.

Response to Arguments

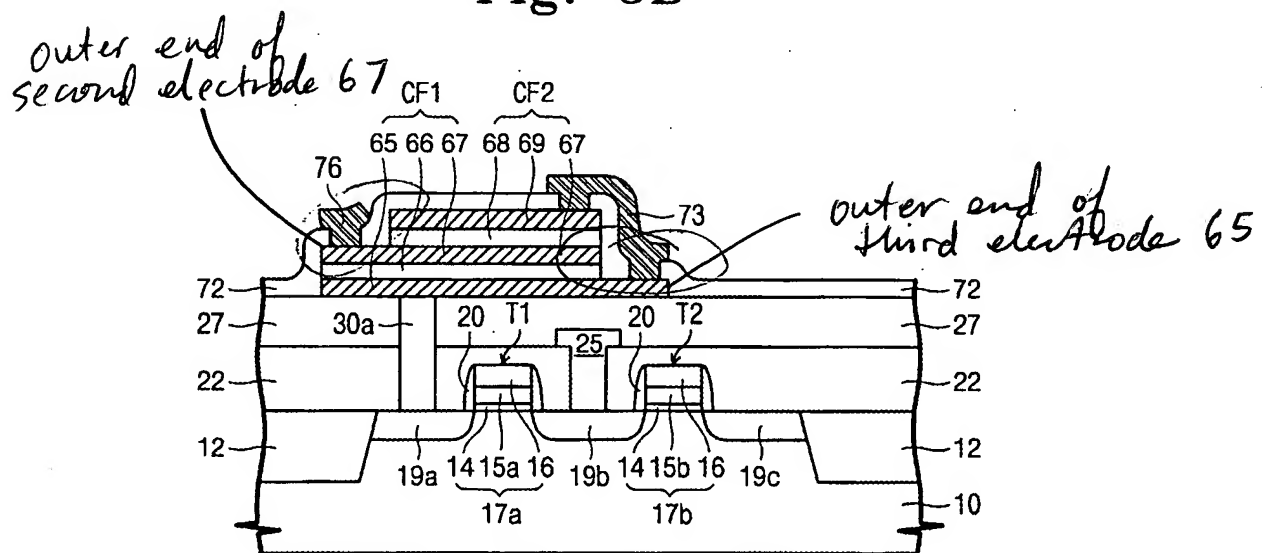
6. Applicant's arguments filed 7/15/05 have been fully considered but they are not persuasive.

Regarding the applicant's argument on page 8, first and second paragraphs of the amendment filed 7/15/05 that Kim fails to teach or suggest "an outer end of the second electrode is entirely positioned outside the first electrode" and further Kim also fails to disclose the claimed "outer end of the third electrode is entirely positioned outside the second electrode" because the right end of middle electrode 67 is not positioned outside upper electrode 69, and the left end of lower electrode 65 is not positioned outside middle electrode 67, this argument is not persuasive. Even though the right end of middle electrode is not positioned outside upper

Art Unit: 2815

electrode, and the left end of lower electrode is not positioned outside middle electrode, these are not the only ends of the middle electrode and the lower electrode. The middle electrode and lower electrode also have a left end and right end respectively, and these ends clearly show the outer end (left end) of the second electrode 67 being entirely positioned outside the first electrode 69, and further the outer end (right end) of the third electrode 65 being entirely positioned outside the second electrode 67. Please see figure below.

Fig. 5B



Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO**

Art Unit: 2815

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
August 4, 2005

